

Ultra-shallow SIMS for semiconductor depth profiling

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In this talk, I will give an overview of the current challenges to silicon CMOS (Complementary Metal-Oxide-Semiconductor) technology scaling, as well as my perspectives on the role of ultra-shallow SIMS depth profiling in the semiconductor industry.

Enabling technologies for ultimate CMOS scaling

Some of the key challenges for Si CMOS conventional device scaling include reducing the equivalent oxide thickness (EOT), effective gate length (L_G), junction depth (x_j); increasing the doping concentration in the shrinking device; and reducing the power supply voltage (V_{DD}) to contain power consumption and reduce the heat load. However, conventional device scaling presents numerous technological challenges. For example, reducing the gate dielectric thickness causes an increase in gate leakage current and gate depletion effects. Reduce the gate length results in short-channel effects, and reducing the junction depth causes an increase in parasitic series resistance. New enabling technologies are being developed to improve performance in CMOS scaling. These include the modification of existing materials properties (e.g. the use of strained-Si to improve carrier mobility), introduction of new materials (e.g. metal-gate/high-k dielectrics, new channel materials), and new device structures (e.g. multiple-gate transistors). Figure 1 shows the current world's smallest transistor with 5 nm gate length, where a germanium stressor is used to create high strain levels in a tiny volume of silicon channel in a transistor, resulting in a significant increase in carrier mobility.

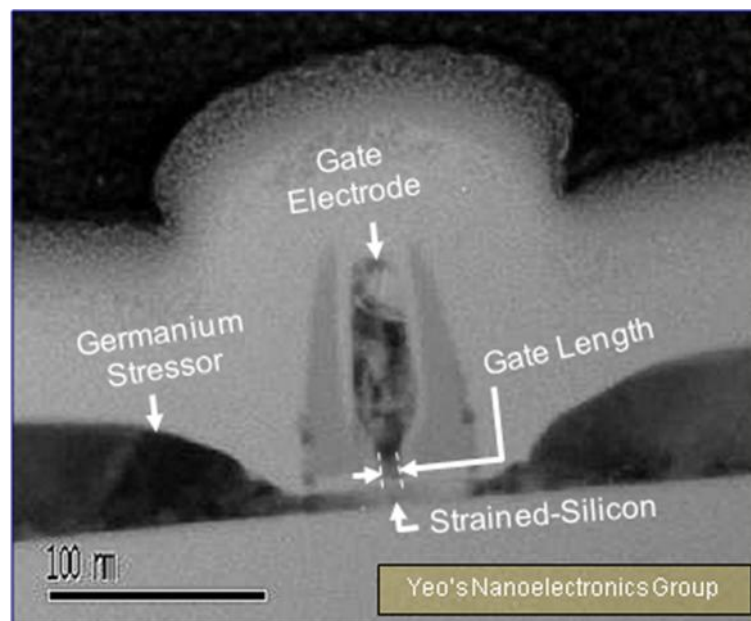


Fig. 1. Strained transistor with 5 nm gate length; first demonstration of germanium stressor to create high strain levels in a tiny volume of silicon channel in a transistor, resulting in a significant increase in carrier mobility. (Courtesy of Y.C. Yeo, presented at VLSI Symp. 2008, Honolulu, HI)

In view of the impressive Si CMOS technology improvements, how will SIMS continue to play an important role in semiconductor dopant depth profiling? Although the SIMS technique has been invaluable to the semiconductor industry due to its high dopant sensitivity (ppm to ppb levels), SIMS has several limitations. The ultimate SIMS lateral resolution is of the order of 100 nm which is much larger than current CMOS structures (such as the source-drain extension), so test structures need to be fabricated on wafers for process monitoring by SIMS. Furthermore, SIMS instrumental effects such as surface transients, surface roughening, and ion beam mixing need to be accounted for, and SIMS data need to be complemented by electrical measurements since SIMS measures the total dopant profile, inclusive of unactivated dopants.

Solutions to surface transient problem

Some of the key challenges to ultra-shallow SIMS profiling are presented by developments in ultra-thin dielectric layers, ultra-shallow dopant profiles and junction depths. Current depth scales required in the profiling of ultra-shallow junctions and ultra-thin gate dielectrics coincide with the surface transient region of SIMS. Many solutions have been developed to address the surface transient issue. Capping the surface allows the surface transient region to be bypassed before the region of interest is profiled [1]. Figure 2 shows that SIMS profiling with a capping layer allows a more accurate N profile close to the top surface of the nitrided gate oxide, which fabricated by decoupled plasma nitridation (DPN).

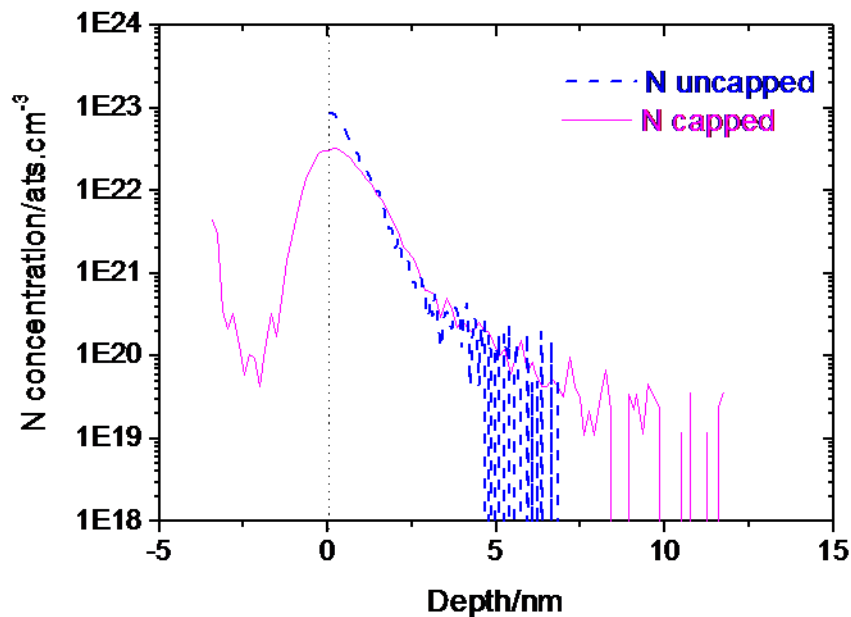


Fig. 2. SIMS depth profiles of silicon oxynitride (SiON) gate dielectric layer, with and without capping with a thin layer of oxide (adapted from Ref [1]).

Profiling the wafer from the backside is another feasible approach to overcoming surface transient and ion beam knock-on effects, especially on SOI (silicon-on-insulator) wafers [2]. The use of lower primary ion impact energy and appropriate incidence angles can minimize the surface transient effect [3-5]. More recently, using the atom probe for 3D dopant profiling is becoming a popular alternative to ultra-shallow SIMS profiling [6].

Low energy SIMS optimal conditions

This challenge for accurate profiling at the near-surface is directly influenced by the probe energy and the angle of incidence of the primary ion used. These two parameters determine the

penetration depth of the primary ion beam and the development of surface roughening. The oxygen matrix effect poses additional problems in quantifying accurate dopant or impurity distributions. By lowering the ion impact energy, the sputter rate and surface transient width in SIMS will be reduced.

We have reported comprehensive studies of surface transient widths, sputter rates and depth resolution as a function of primary ion energy (E_p from 250 eV to 1 keV) and using a wide range of incidence angles ($0 - 70^\circ$), for both oxygen [4,7] and cesium [5,8] primary ions. The instrument used was the Atomika 4500 instrument and the sample was a Si substrate with 10 delta-layers of $\text{Si}_{0.7}\text{Ge}_{0.3}$; a typical depth profile is shown in Figure 3. We observed that the lowest transient width of 0.7 nm is obtainable at normal and near-normal incidence with $E_p \sim 250$ eV and $E_p \sim 500$ eV, with no significant improvement in transient width going down in energy from $E_p \sim 500$ to ~ 250 eV. The onset of roughening is also not obvious at $E_p \sim 250$ eV over the whole angular range studied. Although the sputter rate during the surface transient is normally different from that at steady state, only at $E_p \sim 250$ eV was it observed that the sputter rate remained fairly independent of depth.

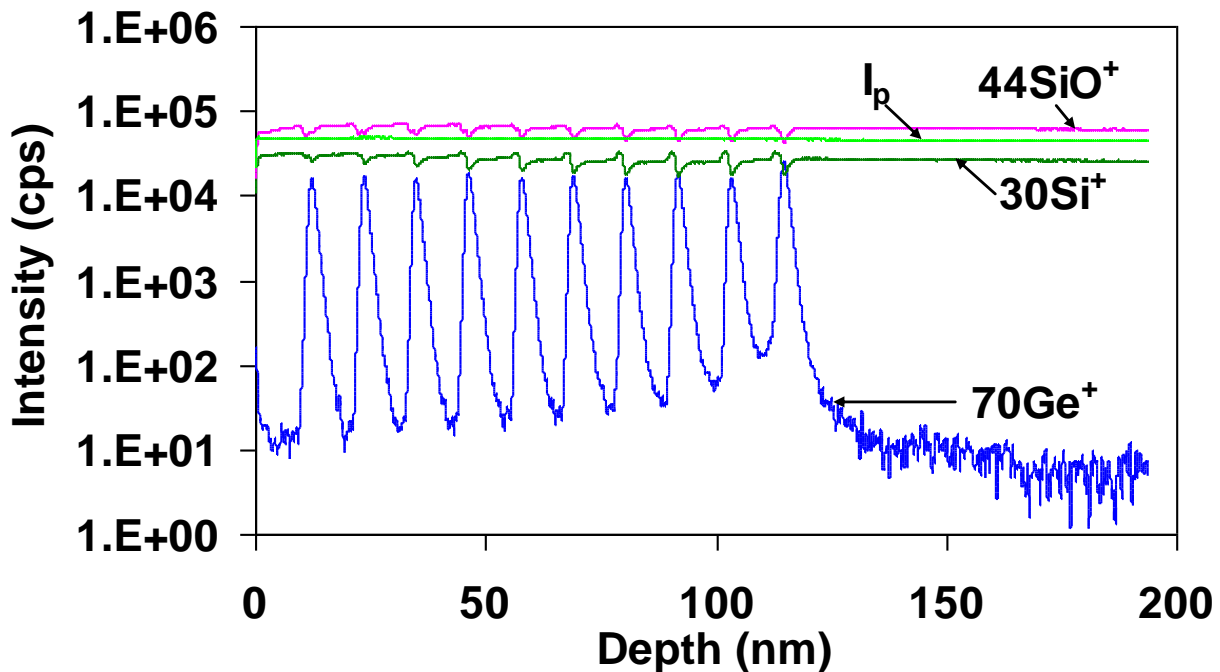


Fig. 3. SIMS depth profile of Ge-delta doped Si sample obtained using O_2^+ primary ion energy $E_p \sim 250$ eV at incidence angle $\theta \sim 20^\circ$ (adapted from Ref [4]).

From our SIMS studies, we propose that the optimum conditions for O_2^+ positive SIMS analysis with the best working range, narrow transient and accurate depth calibration is: $E_p = 250$ eV, $\theta = 0-20^\circ$; or $E_p = 500$ eV, $\theta = 0-10^\circ$. For Cs^+ negative SIMS analysis, the best condition for high depth resolution and good dynamic range is: $E_p = 250$ eV, $\theta = 40^\circ$. We have also investigated the SIMS altered layer at steady state sputtering using *in-situ* XPS to explain the onset of roughening by the presence of a mixed oxide surface in the crater [9].

Oblique incidence SIMS

As the most commonly used SIMS instrument in the semiconductor industry is a magnetic sector SIMS with oblique incidence primary beam, many studies have been done on the use of oxygen flooding and sample rotation to minimize undesirable effects at oblique incidence. We have investigated the effect of oxygen flooding on crater surface composition and surface roughening in

oblique SIMS profiling in a Cameca 6f instrument [10]. Figure 4 shows a plot of SIMS crater bottom roughening as function of oxygen flooding pressure [1]. Oxygen flooding has two competing effects on surface roughening, enhancement of initial roughening and suppression of roughening development. At the intermediate pressure of $\sim 5.8 \times 10^{-5}$ Pa, surface roughening becomes most pronounced. The surface roughening is negligible without flooding or with flooding at saturated oxygen pressure.

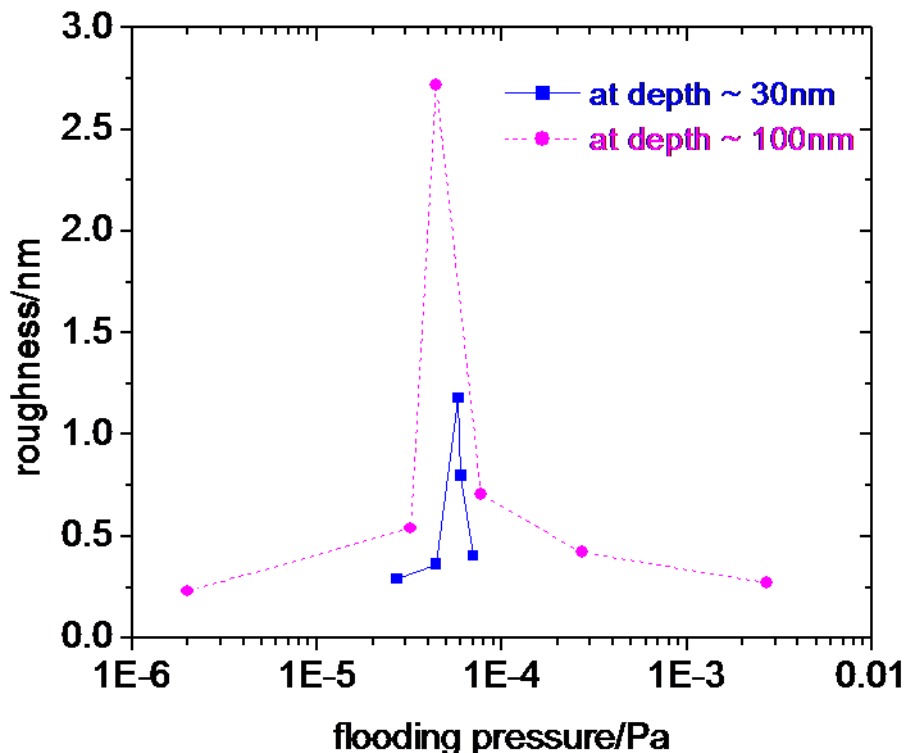


Fig. 4. SIMS crater bottom roughening with oxygen flooding and sample rotation (adapted from Ref [1]).

Beyond Si and III-V: Graphene?

The International Roadmap for Semiconductors (ITRS) 2007 roadmap has recommended the use of new materials to replace the silicon channel when CMOS technology is scaled to and beyond the 16 nm technology generation [11]:

“Develop new materials to replace silicon as an alternate channel to increase the saturation velocity and maximum drain current in MOSFETs while minimizing leakage currents and power dissipation for technology scaled to 16 nm and beyond. Candidate materials include Ge, SiGe, III-V compound semiconductors, and graphene. Develop 1D (nanowire or nanotube) structures to scale MOSFETs and CMOS gates beyond the 16 nm technology generation.”

In particular, graphene (single layer of graphite) may enable novel and complementary applications to carbon nanotubes (CNT), its 1D counterpart. Graphene is receiving considerable attention because it exhibits ambipolar carrier conduction, a carrier mobility as high as $\sim 2 \times 10^6$ cm²/V-sec, and a low defect density of $\sim 1 \times 10^{10}$ /cm². The mobility of graphene is practically independent of temperature, thus opening the possibility of room temperature ballistic transport at the sub-micrometer scale. Graphene on SiC can be patterned and etched by conventional planar lithography techniques and has the best reported transport properties, but processing temperatures of 1200–

1400°C are incompatible with CMOS fabrication. The fabrication of graphene on Si, compatible with current CMOS technology, remains a challenge.

Since electronically interesting graphene is only one (monolayer graphene, MLG) or two (bilayer graphene, BLG) monolayers thick, we have used a range of complementary surface science tools such as scanning tunnelling microscopy (STM), synchrotron photoemission (PES), near edge x-ray absorption fine structure (NEXAFS) and Raman spectroscopy to investigate epitaxial graphene (EG) [12-14]. Figure 5 shows *in-situ* STM images of single-layer and multi-layer epitaxial graphene grown on a 6H-SiC(0001) substrate. Figure 6 shows the corresponding PES and Raman spectra of epitaxial graphene. We show that the transition from monolayer EG to trilayer EG adopts a bottom-up growth mechanism [15]. With the increase in annealing temperature, the fluorescence yield of Si K-edge NEXAFS indicates an increase in disorder of Si atoms in the SiC substrate beneath the surface due to out-diffusion of Si atoms to the surface forming increased Si vacancies [16]. We demonstrate that EG thermally grown on 6H-SiC(0001) can be *p*-doped via a novel surface transfer doping scheme of modifying the surface with the electron acceptor, tetrafluoro-tetracyanoquinodimethane (F4-TCNQ) [17]. The new field of graphene-based devices is still in its infancy, and many exciting possibilities await us.

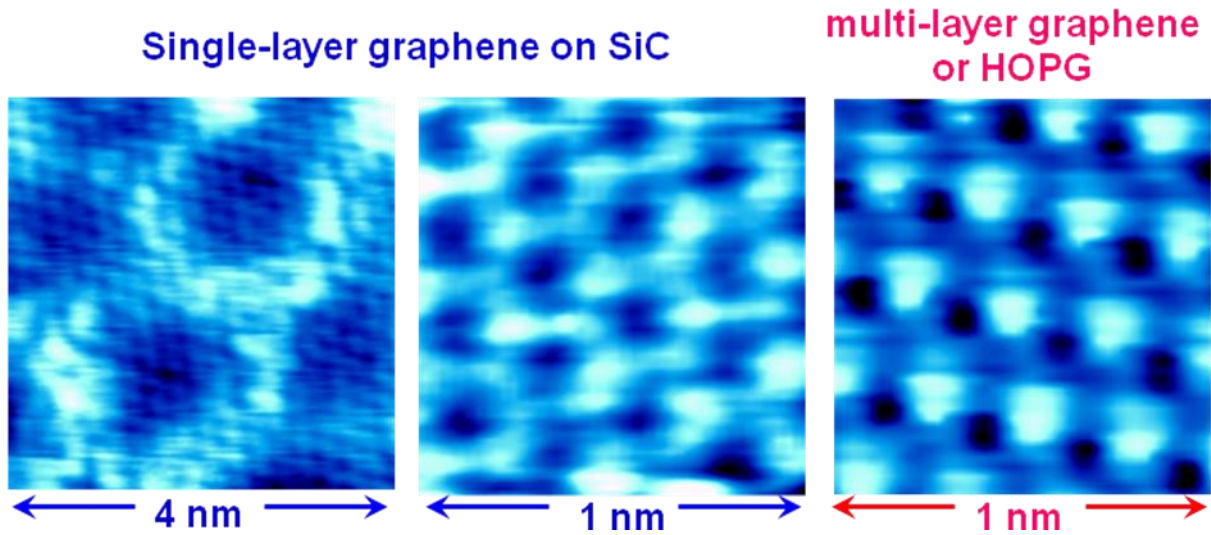


Fig 5. STM images of single-layer and multi-layer epitaxial graphene grown on a 6H-SiC(0001) substrate.

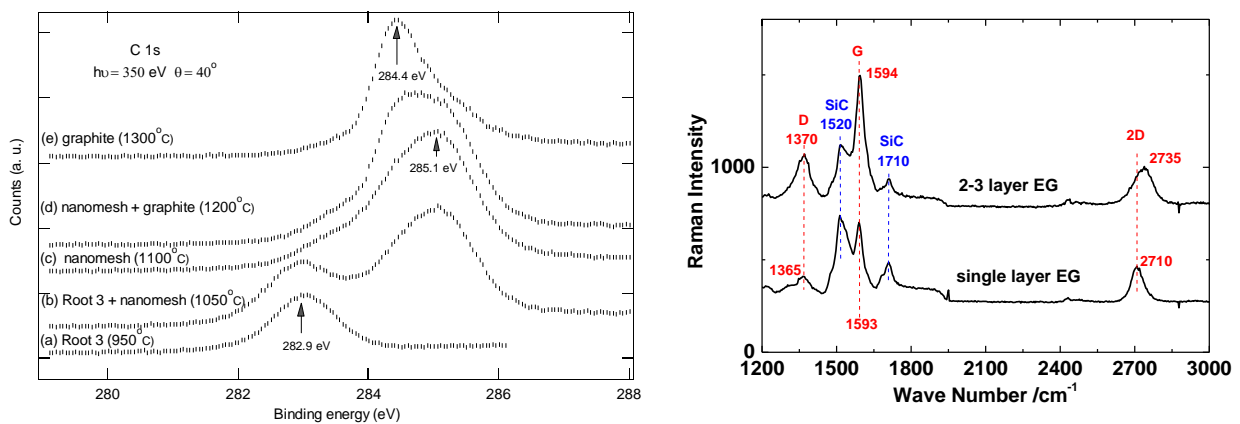


Fig. 6. PES (left) and Raman (right) spectra of epitaxial graphene (adapted from Ref. [12] and [14]).

Future of ultrashallow profiling

It has become clear that the unlimited reduction of the SIMS primary ion energy is not possible as no target atom removal occurs below the threshold energy for sputtering [3]. For O_2^+ , the minimum value for sputtering lies around 30–40 eV, and for Cs^+ the threshold energy for sputtering lies around 100–10 eV. The use of cluster beams does not appear to solve the depth resolution issues and suffers from unexpectedly large decay length values even considering the low energy per constituent atom. Nevertheless, SIMS is still the technique of choice for depth profiling in the semiconductor industry as it is relatively simple, and when reproducibility rather than accuracy is needed for process monitoring. The 3D atom probe can give atomic scale 3D dopant profiling, and is set to become an important tool for the semiconductor industry, particularly in the research and development laboratories where extensive sample preparation capabilities are available. Low energy ion scattering (LEIS) is a promising technique but useful mainly for heavier atoms in a lighter matrix. Angle (and energy) resolved PES has always been an important non-destructive technique for quantitative surface analysis and near surface profiling, and its limitation of lower elemental sensitivity may not be a serious problem as ultra-shallow doping levels now often exceed 10^{20} at/cm³.

In conclusion, with the introduction of new materials to replace silicon (e.g. Ge, SiGe, Si:C, III-Vs, graphene), a combination of complementary surface analysis techniques may be the best way forward for materials characterization in the semiconductor industry.

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